# 1322x-IPB Development Board

Reference Manual

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# About This Book

This manual describes Freescale's 1322x-IPB evaluation board. The 1322x-IPB contains the MC1322x Freescale third-generation ZigBee platform which incorporates a complete, low power, 2.4 GHz radio frequency transceiver, 32-bit ARM7 core based MCU, hardware acceleration for both the IEEE 802.15.4 MAC and AES security, and a full set of MCU peripherals into a 99-pin LGA Platform-in-Package (PiP). This evaluation board design/layout is intended as a reference design for use by MC1322x applications.

## Audience

This manual is intended for system designers.

## Organization

This document is organized into four chapters.

| | |
|---|---|
| Chapter 1 | 1322x-IPB Module Overview and Description — This chapter introduces the 1322x-IPB which is a reference design based on the MC1322x device that demonstrates a very small footprint, 2-layer module. |
| Chapter 2 | Board Overview and Usage — This section provides a system and design overview of the 1322x-IPB and also some usage considerations. |
| Chapter 3 | Schematic and Bill of Material — Provides a schematic and Bill of Materials. |
| Chapter 4 | PCB Manufacturing Specifications — This chapter provides the specifications used to manufacture the 1322x-IPB Printed Circuit Board (PCB). |

## Revision History

The following table summarizes revisions to this document since the previous release (Rev 0.0).

**Revision History**

| Location | Revision |
|---|---|
| Chapter 4<br>Chapter 2 | Added PCB build information<br>Extensive rewrite |

# Chapter 1
# 1322x-IPB Module Overview and Description

Freescale provides a series of cost-effective, small footprint devices for IEEE 802.15.4 and ZigBee applications. To assist the user in producing a quick and successful design, Freescale also supplies the 1322x-IPB which is a reference design based on the MC1322x device that demonstrates a very small footprint, 2-layer module and use of a low cost printed “F” antenna, low power consumption. The heart of the 1322x-IPB is Freescale’s MC1322x, which incorporates a complete, low power, 2.4 GHz radio frequency transceiver, 32-bit ARM7 core based MCU, hardware acceleration for both the IEEE 802.15.4 MAC and AES security, and a full set of MCU peripherals into a 99-pin LGA Platform-in-Package (PiP)..

## 1.1 Introduction

The 1322x-IPB IEEE 802.15.4/ZigBee wireless node module represents a complete IEEE 802.15.4/ZigBee wireless node reference design. The printed circuit board (PCB) has a very small form factor and emphasizes the use of a printed “F” antenna and a layout using only 2 metal layers. A single 802.15.4 device (the MC1322x) is the only required IC and the required RF circuitry is minimal. A single port connector provides power and I/O including a serial I2C bus interface, a separate UART interface, and an ADC analog input.

Freescale provides the 1322x-IPB as a complete reference design with circuit schematic, bill of materials (BOM), and layout database. This reference design can be used “as-is” or can be adapted for small footprint boards, especially if a chip antenna is desired.

**NOTE**

Depending on design needs, Freescale also provides an alternative small footprint reference board design. The user can determine which design best meets their needs:

- The 1322x-IPB solution (this manual) uses a 2-layer PCB with a printed wire “F” antenna providing better RF performance and has a larger footprint.
- The 1322x-ICB solution (the alternative) also uses a 2-layer PCB but uses a chip antenna for a smaller footprint while sacrificing some RF performance.

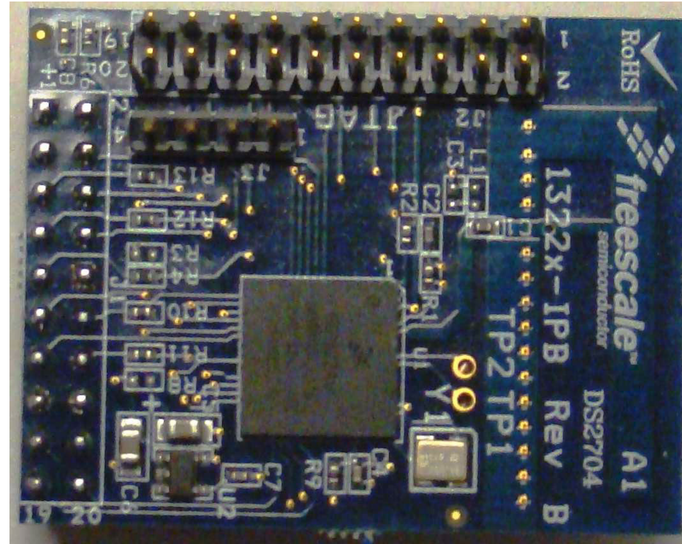


Figure 1-1. 1322x-IPB IEEE802.15.4 Wireless Module

## 1.2 Features

The 1322x-IPB provides the following features:

- Full IEEE 802.15.4 compliant wireless node; ZigBee capable with Freescale's BeeStack software stack
- Based on Freescale's MC1322x transceiver that incorporates a complete, low power, 2.4 GHz radio frequency transceiver, 32-bit ARM7 core based MCU, hardware acceleration for both the IEEE 802.15.4 MAC and AES security, and a full set of MCU peripherals into a 99-pin LGA Platform-in-Package (PiP).
- PCB only requires 2 metal layers
- Provides a highly integrated, low cost RF node
  - — Typical -96 dBm sensitivity
  - — Typical 0 dBm output power, with max approximately +4.0 dBm
  - — Printed metal "F" antenna
- Complete reference design with database

## 1.3 Board Level Specifications

**Table 1-1. 1322x-IPB Specifications**

| Parameter | | | | Units | Notes/Conditions |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **General** | | | | | |
| Size (PCB: X, Y) | | | 32 x 40<br>1.3 x 1.6 | mm/<br>inches | |
| Layer build (PCB) | | 0.8/<br>0.032 | | mm/<br>inches | 2-Layer |
| Dielectric material (PCB) | | | | | FR4 |
| **Power** | | | | | |
| Voltage supply<br>With Onboard regulator<br><br>Bypass onboard regulator | <br>3.65<br><br>2.0 | <br><br><br>3.0 | <br>16.0<br><br>3.6 | <br>V | <br>Determined by the voltage regulator input specification<br>Determined by the MC1322x specification |
| Current consumption<br><br>Transmit (modulated, nominal)<br>Receive (continuous) | | <br><br>21<br>24 | | <br><br>mA | System (board-level) currents measured at VCC_Input<br>CPU on at 2 MHz<br>CPU on at 2 MHz |
| **Temperature** | | | | | |
| Operating temperature | -40 | | +85/+105 | °C | The MC1322x is specified for +105°C. Components on the board must also be specified for this higher temperature if the design is to be used beyond +85°C |
| Storage temperature | -55 | | +125 | °C | |
| **User Interfaces** | | | | | |
| 20-Pin I/O interface & power port | | | | | Supports SPI, serial I2C port, UART port, analog ADC input, Timer port, KBI, reset and supplies power to board (Refer to Section 2.4.2, "I/O Interface & Power Connector (J1)") |
| 20-Pin JTAG debug port | | | | | A standard 20-pin JTAG connector for ARM is connected to the TDI, TMS, TCK, TDO, and RTCK signals of the MC1322x. |
| **RF** | | | | | |
| Frequency range | 2405 | | 2480 | MHz | All 16 802.15.4 channels in the 2450 MHz band, 5 MHz spacing |
| Range (outdoor / line of sight) | | TBD | | Meter | |
| **RF Transmitter** | | | | | |
| Output power range | -30 | 0 | +4.0 | dBm | |
| **RF Receiver** | | | | | |

**Table 1-1. 1322x-IPB Specifications (continued)**

| Parameter | | | | Units | Notes/Conditions |
|---|---|---|---|---|---|
| Sensitivity | | -96<br>-100 | | dBm | Using DCD mode (<1% PER, 20-byte packets)<br>Using NCD mode (<1% PER, 20-byte packets) |
| **Regulatory Approval** | | | | | |
| FCC | | | | | Capable of compliance[1] with the FCC part 15 standard |
| **Environment** | | | | | |
| RoHS[1] | | | | | Capable of compliance[1] with the EU Directive 2002/95/EC of 27 January 2003 |

[1] This design is capable of compliance with the referenced standard, but Freescale does not guarantee nor assume responsibility for a user's compliance to referenced standard.

# Chapter 2
# Board Overview and Usage

This section provides a system and design overview of the 1322x-IPB and also some usage considerations.

## 2.1 Design Overview

The 1322x-IPB design is intended to showcase a small footprint, 2-layer PCB IEEE 802.15.4 wireless node with ZigBee capability based on the MC1322x transceiver.

The main emphasis of the 1322x-IPB module is its low power consumption, 2-layer PCB layout, and low cost printed “F” antenna. The external RF circuitry for the MC1322x is minimal because it uses an onboard balun along with a TX/RX switch allowing direct connection to an external single-ended 50-ohm antenna to complete the radio. This design uses a printed metal “F” antenna to achieve a relatively small area and very low cost RF layout. This creates an excellent reference design for use of an “F” antenna in a 802.15.4 wireless node.

The design (circuitry and layout) may be used directly in a customer’s target design, or it may also be used as a starting point for a compact circuit layout utilizing a printed F antenna. Freescale provides a complete design base including hardware reference manual, data sheets, circuit schematic, BOM, and layouts for customer use.

## 2.2 System Block Diagram

The following is the 1322x-IPB system level block diagram.

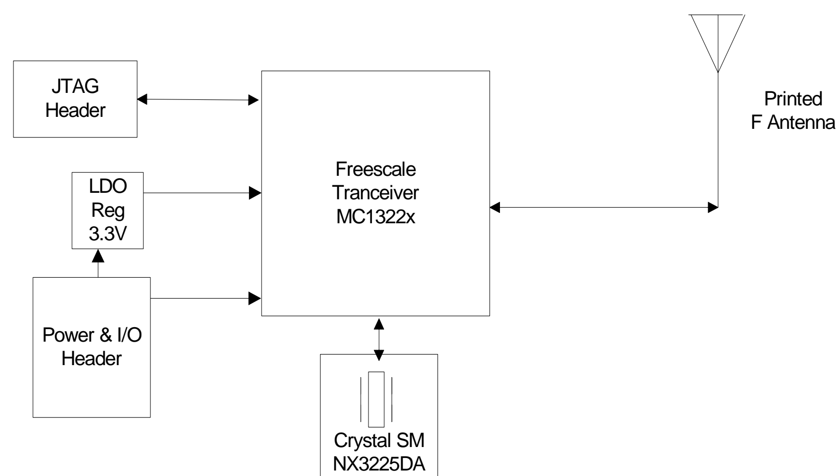


**Figure 2-1. 1322x-IPB Block Diagram**

## 2.3 Form Factor and Layout

This section describes the 1322x-IPB form factor, RF performance, and layout considerations.

### 2.3.1 1322x-IPB Form Factor

The following characteristics have been implemented for the 1322x-IPB board.

- Small footprint
- Printed F antenna
- 2-Layer PCB layout

The MC1322x allows for small footprint application designs and provides the ability for the final solution to fit typical low-power products.

**NOTE**

Use only a properly specified or recommended 24 MHz reference oscillator crystal. See Freescale application note AN3251, *Reference Oscillator Crystal Requirements for the MC1319x, MC1320x, MC1321x, and MC1322x.*

### 2.3.2 RF Performance and Considerations

The MC1322x IEEE 802.15.4 fully-compliant transceiver provides a complete 2.4 GHz radio with 250 kbps Offset-Quadrature Phase Shift Keying (O-QPSK) data in 5.0 MHz channels and full spread-spectrum encode and decode. The modem supports transmit, receive, clear channel assessment (CCA), Energy Detect (ED), and Link Quality Indication (LQI) as required by the 802.15.4 Standard.

- Programmable output power — 0 dBm nominal output power, programmable from -30 to +4 dBm
- Receive sensitivity (at 1% PER, 20-byte packet)
  - < -96 dBm (typical) DCD receive (well below IEEE 802.15.4 specification of -85 dBm)
  - < -100 dBm (typical) NCD receive (higher current consumption in this mode)
- Single-ended 50-Ω antenna port — Uses integrated transmit/receive (T/R) switch, LNA, and onboard balun. Impedance matching onboard.
- Maximum flexibility — Optionally, single-ended port becomes RF input only and a separate set of full differential PA outputs are provided. Separate input and outputs allow for a variety of RF configurations including external LNA and PA for increased range
- Four control signals for external RF components such as a LNA or PA
- Regulated voltage source for PA biasing and powering external components

The RF radio interface provides for low cost solution as shown in Figure 2-1. The single-ended 50-Ω printed F antenna connects directly to the RF Rx_Tx port of the MC1322x radio. If required, external components can be used to provide out-of-band signal suppression.

**NOTE**

Refer to Freescale application note AN2731, *Compact Integrated Antennas Designs and Applications for the MC1319x, MC1320x, and MC1321x* for more information on using antennas.

### 2.3.3 Layout Usage and Recommendations

The RF performance of a 2.4 GHz radio and circuitry can be severely impacted by layout geometries, device placement and board characteristics including dielectric thickness. Freescale provides a one-stop approach to guide customers with their wireless solutions to help minimize product time-to-market. The 1322x-IPB is an example in that all required documentation and design information is provided. It is recommended that the MC1322x PCB and RF layout (including printed F antenna) are best used exactly as provided. Common practice is to use the provided layout for the MC1322x device and the RF components/circuitry. The user can then add his/her circuitry away from the MC1322x device as required.

As changes are required, Freescale recommends following the layout application guidelines in, the *Freescale IEEE 802.15.4 / ZigBee Package and Hardware Layout Considerations Reference Manual* (ZHDCRM). This manual describes Printed Circuit Board (PCB) footprint guidelines for the MC1322x LGA99 package. Included are layouts of the component copper layer, solder mask, and solder paste stencil.

## 2.4 User Interfaces

The 1322x-IPB provides two user interface connectors and a 4-pin FLASH erase header

### 2.4.1 JTAG Debug Connector (J2)

The MC1322x supports connection to a subset of the defined ARM JTAG connector. The JTAG hardware interface uses a 20-pin header (J2) with a standard 0.1 inch spacing. Table 2-1 shows how the MC1322x pins are connected to the associated JTAG header.

**Table 2-1. ARM JTAG 20-Pin Connector J2 Pin Assignments**

| Name[1] | Pin # | Pin # | Name |
|---|---|---|---|
| VBATT/VREG | 1 | 2 | VBATT/VREG |
| NC[2] | 3 | 4 | GND |
| TDI | 5 | 6 | GND |
| TMS | 7 | 8 | GND |
| TCK | 9 | 10 | GND |
| RTCK | 11 | 12 | GND |
| TDO | 13 | 14 | GND |
| RESET[3] | 15 | 16 | GND |

**Table 2-1. ARM JTAG 20-Pin Connector J2 Pin Assignments (continued)**

| Name[1] | Pin # | Pin # | Name |
|---|---|---|---|
| NC | 17 | 18 | GND |
| NC | 19 | 20 | GND |

[1] NC = No Connect.
[2] MC1322x does not support separate JTAG reset TRST.
[3] VBATT through a 100k-Ω pullup.

### 2.4.2 I/O Interface & Power Connector (J1)

Table 2-2 shows the pinout connections for the I/O Interface & Power port (J1). The schematic in Chapter 3, "Schematic and Bill of Material" shows the detailed connections to the interface.

**NOTE**

Interface signal voltages must match the modem of the IPB supply voltage:

- If the voltage regulator is used, the I/O interface should be referenced to 3.3 volts.
- If the voltage regulator is bypassed, the I/O interface should be referenced to the VIN input voltage.
- If the MC1322x is put into low power mode, all non-KBI signals must be driven low.

**Table 2-2. I/O and Power 20-Pin Connector J1 Pin Assignments**

| Name | Pin # | Pin # | Name |
|---|---|---|---|
| VIN | 1 | 2 | SPI_SS |
| GND | 3 | 4 | SPI_MOSI |
| UART1_TX | 5 | 6 | SPI_MISO |
| UART1_RX | 7 | 8 | SPI_CLK |
| ADC0 | 9 | 10 | RESETB |
| I2C_SDA | 11 | 12 | UART1_RTS |
| I2C_SCL | 13 | 14 | UART1_CTS |
| GND | 15 | 16 | TMR1 |
| KBI_4 | 17 | 18 | KBI_5 |
| KBI_6 | 19 | 20 | KBI_7 |

**NOTE**

This IPB reference manual makes no attempt to provide applications information for use of the MC1322x. The user is advised to reference the following documents:

- Freescale *MC13224V Technical Data,* Doc No. MC1322x
- Freescale *MC1322x Reference Manual,* Doc No. MC1322xRM

The I/O connector supports the following interfaces

- Input Supply voltage (VIN) - DC supply voltage to the module
  - The onboard 3.3V regulator can be used resulting in an allowable input voltage of 3.65V to 16V
  - The onboard regulator can be eliminated or bypassed resulting in an allowable input voltage of 2.0V to 3.6V as determined by the MC1322x specification
- I2C Bus serial port
  - Signals I2C_SDA and I2C_SCL
  - Pullup resistors are not provided
- UART serial port
  - Signals UART1_TX, UART1_RX, UART1_CTS and UART1_RTS
  - Flow control signals UART1_CTS and UART1_RTS are hardware controlled
- SPI serial port - Signals SPI_MOSI, SPI_MISO, SPI_CLK and SPI_SS
- Four KBI signals
  - KBI_4, KBI_5, KBI_6 and KBI_7
  - Can be used as GPIO
  - Revert to powered inputs when MC1322x is in reset or low power mode; can be used for wake-up
- Single analog ADC input - Signal ADC0 can be used as GPIO and ADC input
- Timer control signal - Signal TMR1 can be used as GPIO, timer input or output, or a test point to calibrate reference oscillator
- Reset - Signal RESETB is an asynchronous device reset input (active low)

### 2.4.3 4-Pin FLASH Erase Header (J3)

The MC1322x has an onboard serial FLASH that stores the memory image that gets loaded into RAM at boot. If it becomes necessary to change or update the image in FLASH, the 1322x-IPB has a 4-pin header (J3) (see Figure 2-2) that must be used to erase the FLASH:

1. Short Pin 1 to Pin 2 with a shorting bar, as well as, short Pin 3to Pin 4 with a second shorting bar.
2. Turn on power, cycle the RESETB signal (assert low then release high), and wait a few seconds.
3. Turn off power and remove the jumper bars.
4. The board is now ready for boot operation.

After the FLASH is erased, the module can be loaded with a new image.

**NOTE**

Refer to the *MC1322x Reference Manual*, Chapter 3 for information on the MC1322x boot flow and FLASH erase mechanism.

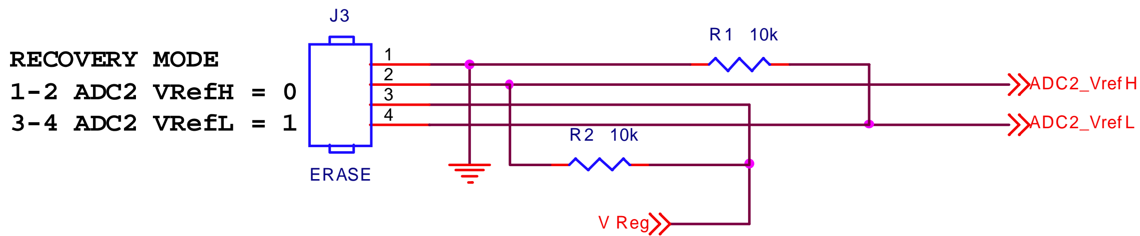


Figure 2-2. FLASH Erase Header J3

## 2.5 Software Support (Building a 1322x-IPB Project in BeeKit)

In addition to the complete hardware database and supporting documentation, the provided downloadable material includes a configuration platform file (`1322x-IPB_Platform.bkudp32`) that allows the design to be easily supported by Freescale's BeeKit Wireless Connectivity Toolkit .

This section describes how to create a MAC endpoint device employing a user defined target configuration and importing the corresponding platform editor configuration file into the platform editor in BeeKit. For more information about MAC applications, see the Freescale *802.15.4 MAC MyWireless Application User's Guide or 802.15.4 MAC MyStarNetwork Application User's Guide.* For more information about BeeKit, see the *BeeKit Wireless Connectivity Toolkit User's Guide*.

1. Launch BeeKit.
2. Click on File -> Select Codebase.
3. Then select the `ARM7 MAC codebase (version)`
4. Click on -> Set Active.
5. Click on File ->New Project.
6. Complete the following:
   a) Then select an appropriate template for the end point (for this example, `MyWirelessApp Demo Non Beacon (End Device)`).
   b) Enter an appropriate Project Name (use the default for this example)
   c) Solution Name (use default)
   d) Location for the new project (Pick a desired directory or use the default).
7. Click on OK.
   a) The Welcome Screen of the BeeKit Project Configuration Dialog appears.
   b) The Welcome Screen displays a snap-shot of the current projects defaults settings. On the left side, it also lists all the editable features and their parameters that can be changed for the project if desired. In addition, the Welcome Screen describes the next steps to follow.
   c) Click on 'Select Hardware' from the list on the left side of the Welcome Screen.
8. Choose 'User defined target' configuration.

9. Click on Finish.
10. In the Solution Explorer window, expand the project and select Platform.
11. In the Property List tab window, scroll down to a selectable field header under `PortConfig.h` (for example GPIO Direction Register Low) and select that field by clicking on it.

    An icon with three dots to the right of the value field appears.
12. Click this icon. The Platform Editor window will now open allowing the users to load their Configuration File.
13. In the Platform Editor window, click on the ‘Load Configuration From File’ button.
14. Navigate to the folder containing the `1322x-IPB_Platform.bkudp32` platform file, select the file and click the OK button.
15. From the Solution menu, select ‘Export and Open Solution in IAR EWB’.
16. Select the project just created and click on OK.
17. Close BeeKit.

The BeeKit project is now imported and opened in IAR EWB and ready to be built and downloaded to a 1322x-IPB end point device as described in the appropriate Freescale 802.15.4 MAC and/or BeeKit documentation.

**NOTE**

Errors can be incurred during the importing process of the BeeKit Solution into IAR EWB if there are version differences with the `_Platform.bkudp32` platform file and IAR version.

# Chapter 3
# Schematic and Bill of Material

## 3.1 Schematic

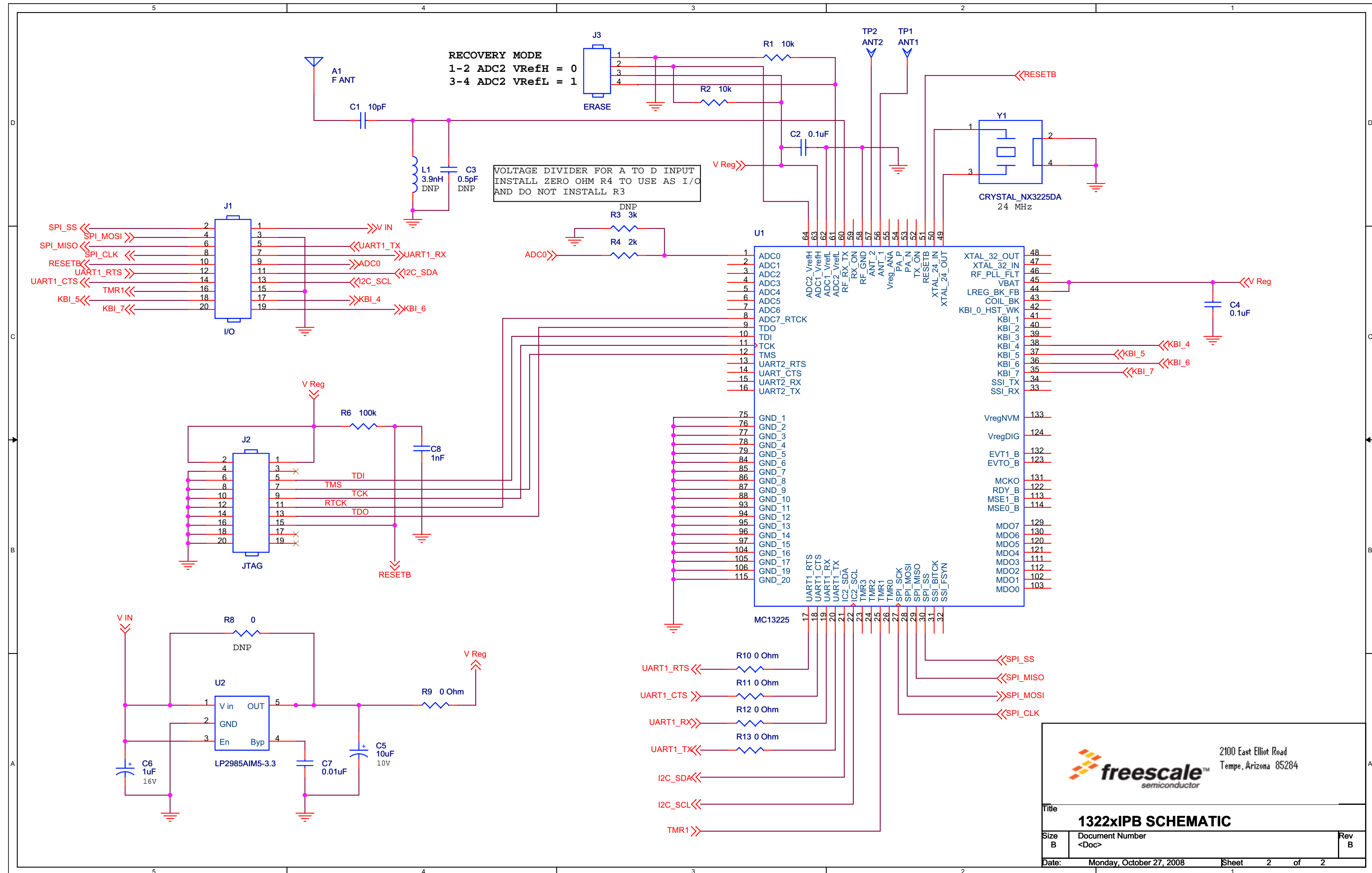


Figure 3-1. 1322x-IPB Schematic

## 3.2 Bill of Materials

**Table 3-1. Bill of Material**

| Qty | Part Reference | Description | Value | Manufacturer | Manufacturer Part Number |
|---|---|---|---|---|---|
| 1 | A1 | Printed F ANT. | | | |
| 6 | C1,C2,C5,C6,C12,C13 | Capacitor | 0.1uF | Venkel | C0402X7R500-104KNE |
| 2 | C3,C4 | Capacitor | 8pF | Venkel | C0402COG500-8R0CNE |
| 1 | C8 | Capacitor | 0.5pF | Venkel | C0402COG500-0R5BNE |
| 1 | C9 | Capacitor | 1.8pF | Venkel | C0402COG500-1R8BNE |
| 2 | C15,C16 | Capacitor | 10pF | Venkel | C0402X5R500-100CNE |
| 1 | C17 | Capacitor | 1.0uF | Venkel | TA016TCM-105KAR |
| 1 | C18 | Capacitor | .01uF | Venkel | C0402X7R500-103KNE |
| 1 | C19 | Capacitor | 10uF | Venkel | TA010TCM-106KAR |
| 1 | D1 | G LED | | Avago | HSMG-C190 |
| 1 | J1 | Power & I/O | Header 1x8 | Tyco | 9-146281-0-08 |
| 1 | J2 | BDM | Header 2x3 | Tyco | 9-146261-0-03 |
| 2 | L1,L2 | Inductor | 3.3nH | Venkel | LMCI1005-3N3JT |
| 1 | L3 | Inductor | 8.2nH | Venkel | LMCI1005-8N2JT |
| 1 | R7 | Resistor | 470k | Venkel | CR0402-16W-474JT |
| 1 | R8 | Resistor | | Venkel | CR0402-16W-331JT |
| 5 | R9,R10,R11,R12,R14 | Resistor | | Venkel | CR0402-16W-000T |
| 1 | R13 | Resistor | 47k | Venkel | CR0402-16W-473JT |
| 1 | T1 | Balun | 50/50 Ohm | Johanson | 2050BL15B050 |
| | Suitable Substitute | Balun | Balun 50/50 | Murata | LDB212G4005C-001 |
| 1 | U2 | LDO | Reg.3.3v | National | LP2985AIM5-3.3 |
| | Suitable Substitute | LDO | Reg 3.0v | TI | TPS76430DBVT |
| 1 | U3 | Transceiver | | Freescale | MC1322x |
| 1 | Y1 | Crystal SM | | NDK | NX3225SA-24MHz (for OA/AV and Bluetooth) / S1-3085-1510-9 |

# Chapter 4
# PCB Manufacturing Specifications

This chapter provides the specifications used to manufacture the 1322x-IPB Printed Circuit Board (PCB).

The 1322x-IPB PCB must comply with the following:

- The PCB must comply with Perfag10/3C (http://www.perfag.dk/Uk/ukindex.htm)
- The PCB manufacturer's logo is required
- The PCB production week and year code is required
  - The manufacturer's logo and week/year code must be stamped on the back of the PCB solder mask
  - The PCB manufacturer can not insert text on the PCB either in copper or in silk-screen without written permission from Freescale Semiconductor, Inc.
- The required Underwriter's Laboratory (UL) Flammability Rating level is 94V-0 (http://www.ul.com/plastics/flame.html)
  - The UL information must be stamped on the back of the PCB solder mask

## 4.1 Single PCB Construction

This section describes individual PCB construction details.

- The PCB is a two layer design
- The PCB contains no blind, buried, or micro vias
- Printed Circuit Board data:
  - Size: Approximately 40 x 32 mm (1.3 x 1.6 inches)
  - PCB final thickness (Cu/Cu): 0.8 mm +/- 10% (0.032 mils) (excluding solder mask)

The following table defines each layer of the completed PCB. The artwork identification refers to the name of the layer in commonly used terms.

**Table 4-1. Layer by Layer Overview**

| Layer | Artwork Identification | File Name |
|---|---|---|
| 1 | Solder Resist | `1322x_IPB REVB.SMT` |
| 2 | Copper Top Layer | `1322x_IPB REVB.TOP` |
| 3 | Copper bottom Layer | `1322x_IPB REVB.BOT` |
| 4 | Solder Resist | `1322x_IPB REVB.SMB` |

- Solder mask is required
- Silk screen is required

## 4.2 Panelization

The panel size can be negotiated depending on production volume.

## 4.3 Materials

### 4.3.1 Laminate

The base material (laminate) must meet the following requirements:

- Base laminate material: FR4
- Laminate thickness: 0.762 mm, 30 mils.

### 4.3.2 Copper Foil

The copper foil (Top and Bottom layers) must be 1 oz. copper

### 4.3.3 Plating

All pad plating must be Hot Air Levelling (HAL)

## 4.4 Solder Mask

The solder mask must meet the following requirements:

- Solder mask type: Liquid Film Electra EMP110 or equivalent
- Solder mask thickness: 10–30 µm

## 4.5 Silk Screen

The silk screen must meet the following requirements:

- Silkscreen color: White
- Silkscreen must be applied after application of solder mask if solder mask is required
- The silkscreen ink must not extend into any plated-thru-holes
- The silk screen must be clipped back to the line of resistance

## 4.6 Electrical PCB Testing

All PCBs must be 100 percent tested for opens and shorts

## 4.7 Packaging

- Finished PCBs must remain in panel
- Finished PCBs must be packed in plastic bags that do not contain silicones or sulphur materials. These materials can degrade solderability

## 4.8 Impedance Measurement

An impedance measurement report is not mandatory.

## 4.9 Hole Specification/Tool Table

See file `1322x_IPB REVB.DRD`

## 4.10 File Description

Refer to the text file included with the Gerber files for the file names and descriptions.

- Data Format — Extended Gerber format RS-274x